IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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		)	Examiner: M. Tran
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Entitled: 256 MEG DYNAMIC RANDOM ACCESS MEMORY

Complete Clean Set Of Claims Currently Pending

444. (Amended) A device responsive to first and second external signals for controlling a power up of a first voltage supply, comprising:

a first circuit responsive to the first external signal for producing a first output signal indicative of whether the first external signal is greater than a first predetermined voltage; and

a second circuit responsive to the first output signal and the second external signal for producing a first enable signal to enable the first voltage supply.

445. The device of claim 444, wherein said first predetermined voltage is approximately two volts.

446. The device of claim 444, wherein said first circuit includes:

a first voltage detector responsive to the first external signal for producing a first signal indicative of the first external signal being greater than said first predetermined voltage;

a second voltage detector responsive to the first external signal for producing a second signal indicative of the first external signal being greater than said first predetermined voltage; and

a logic circuit responsive to said first and second signals for producing said first output signal.

a resistor having a first end and a second end, said first end in communication with a reference potential;

a plurality of series-connected, n-channel transistors each having a gate terminal in communication with the first external signal, with one of said transistors having a drain terminal in communication with the first external signal, and another of said transistors having a source terminal in communication with said second end of said resistor for producing the threshold signal, said transistors being capable of being shorted across their source and drain terminals to change the value of said threshold signal.

454. The device of claim 453, wherein said signal generating circuit includes:

a resistor having a first end and a second end, said first end in communication with the first external signal; and

an n-channel transistor having a source terminal in communication with the reference potential, a gate terminal in communication with said threshold signal, and a drain terminal in communication with said second end of said resistor for producing said second signal.

455. The device of claim 446, wherein said logic circuit includes:

first and second series connected inverters for receiving said first signal;

a third inverter for receiving said second signal;

a NAND gate responsive to said series connected first and second inverters and said third invertor; and

a fourth inverter responsive to said NAND gate for producing said first output signal.

456. (Twice Amended) The device of claim 444, additionally comprising a reset circuit interposed between said first and second circuits for receiving said first output signal from said first circuit and for terminating said first output signal when predetermined stability requirements are not met.

457. The device of claim 456, wherein said predetermined stability requirements include said first output signal remaining within a predetermined range for approximately one hundred nanoseconds.

458. The device of claim 456 wherein said reset circuit includes:

a plurality of series-connected buffer gates with a first one of said buffer gates responsive to said first output signal; and

a logic circuit responsive to said first output signal and a last one of said series-connected buffer gates.

459. The device of claim 458, wherein said reset circuit includes:

a NAND gate having a first input terminal in communication with said first output signal, a second input terminal in communication with said last one of said series-connected buffer gates, and an output terminal; and

an inverter having an input terminal in communication with said output terminal of said NAND gate, and an output terminal at which said first output signal is available.

460. The device of claim 458 wherein said reset circuit further includes a reset logic gate responsive to said first output signal for producing a reset signal for resetting said buffer gates to a predetermined state.

461. (Amended) The device of claim 444, wherein said second circuit includes:

a logic circuit responsive to said first output signal and the second external signal for producing an output signal; and

a latch responsive to said output signal of said logic circuit for producing said first enable signal.

462. The device of claim 461, wherein said logic circuit includes a NAND gate having a first input terminal in communication with said first output signal, a second input terminal in communication with the second external signal, and an output terminal for producing said output signal of said logic circuit.

463. (Amended) The device of claim 444, wherein said device is responsive to a third external signal for controlling the power up sequence of a second voltage supply, said device comprising:

a third circuit responsive to said first output signal, the second external signal, and the third external signal for producing a second enable signal to enable the second voltage supply.

464. The device of claim 463, wherein said third circuit includes:

a logic circuit responsive to said first output signal, the second external signal, and the third external signal for producing an output signal; and

a latch responsive to said output signal of said logic circuit for producing said second enable signal.

465. The device of claim 464, wherein said logic circuit includes:

a NAND gate having a first input terminal in communication with said first output signal, a second input terminal in communication with the second external signal, a third input terminal in communication with the third external signal, and an output terminal for producing said output signal of said logic circuit.

466. A device for controlling the powering up of a first voltage supply, comprising:

a first voltage detector constructed of substantially identical p-channel and n-channel devices for producing a first output signal indicative of a first external signal being greater than a predetermined voltage substantially independently of process variations;

a reset circuit responsive to said first voltage detector for outputting said first output signal when said first external signal is stable;

a logic circuit responsive to said reset circuit and a second external signal; and

a latch responsive to said logic circuit for producing a first enable signal for controlling the powering up of a first voltage supply.

467. The device of claim 466 wherein said reset circuit comprises:

a plurality of series-connected buffers with a first one of said buffers responsive to said first output signal; and

a logic circuit responsive to said first output signal and a last one of said series-connected buffers.

468. The device of claim 467 wherein said reset circuit is constructed such that the first external signal must remain within a predetermined range for approximately one hundred nanoseconds for said logic circuit to output said first output signal.

469. A device for controlling the powering up of a first voltage supply, comprising:

a first voltage detector comprised of p-channel devices for producing a first signal indicative of a first external signal being greater than a first predetermined voltage;

a second voltage detector comprised of n-channel devices for producing a second signal indicative of the first external signal being greater than said first predetermined voltage;

a logic circuit responsive to said first and second signals for producing a first output signal;

a reset circuit responsive to said first output signal;

a logic circuit responsive to said reset circuit and a second external signal; and

a latch responsive to said logic circuit for producing a first enable signal for controlling the powering up of a first voltage supply.

470. The device of claim 469 wherein said reset circuit comprises:

a plurality of series-connected buffers with a first one of said buffers responsive to said first output signal; and

a logic circuit responsive to said first output signal and a last one of said series-connected buffers.

471. The device of claim 470 wherein said reset circuit is constructed such that the first external signal must remain within a predetermined range for approximately one hundred nanoseconds for said logic circuit to output said first output signal.

472. A device for an integrated circuit having a voltage supply responsive to a voltage external to the integrated circuit and generating a feedback signal, said device comprising:

a first circuit portion responsive to the external voltage for producing a first output signal indicative of whether the external voltage is above a predetermined value; and

a second circuit portion responsive to said first output signal and the feedback signal for producing a first enable signal to enable the voltage supply.

473. The device of claim 472, wherein said first circuit portion includes:

a first voltage detector constructed of p-type components and responsive to the external voltage for producing a first signal indicative of the external voltage being greater than said predetermined value;

a second voltage detector constructed of n-type components and responsive to the external voltage for producing a second signal indicative of the external voltage being greater than said predetermined value; and

a logic circuit responsive to said first and second signals for producing said first output signal.

474. The device of claim 472, wherein said second circuit portion includes:

a logic circuit responsive to said first output signal and the feedback signal for producing an output signal; and

a latch responsive to said output signal of said logic circuit for producing said first enable signal.

475. The device of claim 472, additionally comprising a reset circuit interposed between said first and second circuit portions for receiving said first output signal from said first circuit portion and for terminating said first output signal when predetermined stability requirements are not meet.